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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,955	03/31/2004	Jin Jeon	8054-4 CON (LW7020US-1/KY	7235

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EXAMINER	
DUONG, THOI V	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EL

Office Action Summary	Application No.	Applicant(s)	
	10/814,955	JEON, JIN	
	Examiner	Art Unit	
	Thoi V. Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-11 and 13-30* is/are allowed.

6)☒ Claim(s) *31 and 32* is/are rejected.

7)☒ Claim(s) *33-35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/051,701.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed September 06, 2005.

Accordingly, claims 12, 28 and 32 were amended. Currently, claims 1-35 are pending in this application.

Response to Arguments

2. Applicant's arguments with respect to claim 31 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 recites three types of "data electrodes": a data electrode of the data pattern, a data electrode of a second drive transistor of the peripheral region, and a data electrode of the pixel region. Since claim 12 is dependent on claim 1, it is unclear what type of "the data electrode" recited in the claim belongs to; therefore, claim 12 is indefinite for failing to distinctly claim the subject matter.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 31 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Aoyama et al. (Aoyama, USPN 5,294,811).

Re claim 31, as shown in Figs. 1, 2 and 4, Aoyama discloses a substrate 1 comprising:

a gate pattern 2 formed on a pixel region 50 and a peripheral region, the pixel region and the peripheral region being disposed on the substrate 1 (Fig. 2);

an active pattern 5 insulated from the gate pattern 2 to be formed on the gate pattern 2, the active pattern including a semiconductor layer (col. 4, lines 62-68);

a data pattern 6, 7 electrically connected to a portion of the active pattern 5; and

a first insulating interlayer 10 formed on the data pattern, wherein the pixel region includes a plurality of pixels (Fig. 4) and the active pattern 5 is comprised of amorphous silicon (col. 4, lines 48-61).

Re claim 32, as shown in Fig. 4, the pixels respectively include a first transistor 60a, and the peripheral regions include a plurality of driver transistor 61, 62, 63 for driving the first transistor 60a of the pixels (col. 5, line 56 through col. 6, line 26).

Allowable Subject Matter

7. Claim 12 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. Claims 33-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of

the base claim and any intervening claims. See below the reason for allowance of claims 1 and 23.

9. Claims 1-11 and 13-30 are allowed.

The following is an examiner's statement of reasons for allowance: none of the prior art of record fairly suggests or shows all of the limitations as claimed. Specifically,

Re claims 1 and 23, none of the prior art of record discloses, in combination with other limitations as claimed, a substrate (as well as a method for manufacturing the same) comprising:

a first insulating interlayer formed on the data pattern, the first insulating interlayer having a first contact hole for partially exposing the data electrode of the data pattern, a second contact hole for exposing a gate electrode of a first drive transistor of the peripheral region, and a third contact hole for exposing a data electrode of a second drive transistor of the peripheral region; and

an electrode pattern part formed on the first insulating interlayer, the electrode pattern part including a first electrode pattern in contact with a data electrode of the pixel region through the first contact hole, and a second electrode pattern connecting the partially exposed gate electrode of the first drive transistor with the exposed data electrode of the second drive transistor through the second and third contact holes.

Re claims 13 and 28, none of the prior art of record discloses, in combination with other limitations as claimed, a substrate (as well as a method for manufacturing the same) comprising:

a first insulating interlayer formed on the data pattem, the first insulating interlayer including a first contact hole for partially exposing the second electrode, a second contact hole for partially exposing the first electrode of the pixel region, a third contact hole for exposing a gate electrode of a first drive transistor of the peripheral region, and a fourth contact hole for exposing a data electrode of a second drive transistor of the peripheral region; and

an electrode pattern part formed on the first insulating interlayer, the electrode pattern part including a first electrode pattern coupled to a second electrode of the pixel region through the first contact hole, a second electrode pattern coupled to a first electrode of the pixel region through the second contact hole, and a third electrode pattern connecting the exposed gate electrode of the first drive transistor with the exposed data electrode of the second drive transistor through the third and fourth contact holes.

The most relevant reference, USPN 6,738,109 to Jin Jeon, discloses every limitations of the claimed invention. However, this reference is overcome by a terminal disclaimer filed on March 14, 2005.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (571) 272-2293.

Thoi Duong

11/03/2005

ANDREW SCHECHTER
PRIMARY EXAMINER